Fast and Efficient Domain Specific Hardware Design

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LECTURE ABSTRACT

With the breakdown of Dennard's scaling, computer architectures have dramatically changed to meet stringent power budgets. Most Integrated Circuits (ICs) are now complex System-on-Chip (SoC) that have been tailored for a specific application, a.k.a. domain specific hardware architectures. These SoCs include embedded processors, on-chip memory, different types of interfaces and numerous dedicated hardware accelerators. These heterogeneous SoCs are faster and consume orders of magnitude less power than general purpose systems. Unfortunately, the main problem with these complex SoCs is that they are much harder to design and verify.

This seminar presents a path to generate complete domain specific SoCs at the behavioral level. We will show that the proposed flow allows to generate complex domain specific architectures faster and easier by raising the level of VLSI design abstraction from the RT-level to the behavioral level. Three main contributions enable this: First, an automatic bus generator that generates a synthesizable behavioral description of standard on-chip buses. Second, a library of synthesizable APIs that allow any component in the system to send or receive data through the bus. Third, a library of synthesizable behavioral IPs that includes processors, interfaces and multiple hardware accelerators.

SPEAKER BIOSKETCH

Dr. Benjamin Carrion Schafer completed his Ph.D. at the University of Birmingham, U.K. in 2003. He then worked in the Computer Science Department at the University of California Los Angeles (UCLA) as a Postdoctoral Researcher from 2003 to 2004 and joined the School of Electronic Engineering and Computer Science at Seoul National University, Korea, as a Visiting Research Scholar from 2005 to 2007. From 2007 until

September 2012, he was a researcher at the System IP Core Department, Central R&D Centre, NEC Corporation, Kawasaki, Japan. From 2012 to 2016, he worked as an assistant professor at the Department of Electronic and Information Engineering (EIE) at the Hong Kong Polytechnic University, where he established the Design Automation and Reconfigurable Computing Laboratory (DARClab). Since 2016, he works as an associate professor at the Department of Electrical and Computer Engineering at the University of Texas at Dallas. He is the recipient of the Early Career Scheme from the Research Grants Council, Hong Kong.