Defense Announcement

FPGA Prototyping Framework on Arrow SoCKit Board with Xillybus Interface and Standard FIFO

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FPGA has been a popular candidate in hardware acceleration by offloading compute-intensive tasks from the traditional microprocessors. Due to its parallel nature, customized hardware logic modules implemented on FPGAs can be optimized to perform faster and more energy efficient than the software based counterparts, and with its reconfigurability, design optimization does not induce additional NRE in re-tooling or device re-spins as in the case of ASIC designs. Furthermore, a system-on-chip (SoC) architecture that integrates traditional processors with FPGA fabrics enables a hybrid reconfigurable architecture that the FPGA may be re-purposed as needed on the fly. This thesis presents a prototyping framework for FPGA system development on an Arrow SoCKit board. The framework utilizes the Xillybus data transport interface to handle data communications between the on-board ARM processor and the FPGA function modules. The thesis further presents the data communications interface requirements and the timing analysis in data packet transfer between the host processor application and the FPGA.